INTC

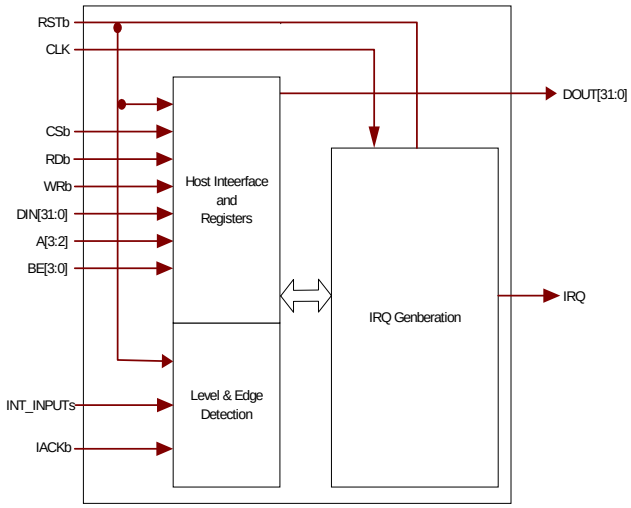
Interrupt Controller (INTC) Intellectual Property (IP).

Description

The interrupt controller (INTC) ascertains the priority of interrupt sources and controls interrupt requests to the CPU. An interrupt is an event that occurs independently of program execution. CPUs can process interrupt requests from the internal peripheral hardware and external sources.

Features

- Number of interrupt inputs is configurable
- Easily cascaded to provide additional interrupt inputs
- Interrupt Enable Register for selectively disabling individual interrupt inputs
- Master Enable Register for disabling the interrupt request output
- Each input is configurable for edge or level sensitivity
  - edge sensitivity can be configured for rising or falling; level sensitivity can be active-high or –low
- Each Interrupt Service is completed Service End Register.
- Fixed Highest Priority and Round Robin Priority.



Application Area : improve system performance by allowing peripheral devices event

Available Documents : Data Sheet, Users Guide
Design File Formats : EDIF File Format , VHDL Code
Verification : Verilog Testbench
Simulation Tool Used : Model Technology ModelSim™ 5.4

For more information

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