

X-DSP

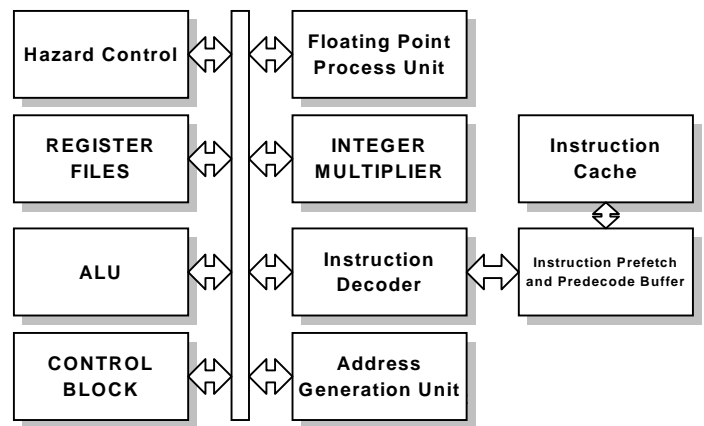
High Performance 32 bit Embedded DSP CORE Intellectual Property (IP).

Description

X_DSP is suitable for the embedded DSP processing application. It has powerful instruction for embedded DSP application. And it has included pipelined floating point and 32 bit multiplier for fast DSP application. It has instruction pre-fetch buffer and pre-decode for fast operation. FPU is fully compatible with IEEE-754. FPU is pipelined multiplier and adder for fast instruction progress. Optimized C compiler is supplied for X-CORE.

Features

- Soft Core.
- 16 Bit Fixed Instruction Set Architecture
- 4 Stage Pipeline (Ultra Low power consumption)
- General Purpose Registers : 32 * 14
- Special Purpose Registers : 32 * 2
- 32 Bit ALSU (includes 32 bit barrel Shifter)
- Little Endian Modes
- Support 4 Co-Processors
- IEEE-754 pipelined floating point processor
- Include instruction pre-fetch buffer and pre-decode for fast operation
- 8 K Bytes 2 way set associative instruction cache
- Performance(MIPS) is depend on the ASIC technology.



Application Area	: Embedded System control, Audio processing, video processing, STB, HDD, Mass storage application
Available Documents	: Data Book, Users Guide, program reference manual
Available Software	: Multi-platform optimized C/C++ Compiler, Assembler, Loader for LINUX, Windows, SUN etc.
Design File Formats	: EDIF File Format , FPGA/ASIC Target NETLIST, VHDL Code
Verification	: Verilog Testbench
Simulation Tool Used	: Model Technology ModelSim™ 5.4

For more information

CROSS S&T Inc. #715 Hyundai Office Bldg. 9-4, Sunae-Dong, Pundan-Ku, Sungnam, Kyunggi-Do, 463-783 Korea

Tel : 82-31-713-9143

Web Site : <http://www.crosssemi.com>

Fax: 82-31-713-9144

Contact To : sales@crosssemi.com

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